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Design high performance Latch for high speed mixed circuit

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Abstract

This article is designing the latch with two inputs and outputs for high speed application. The duty of latch is store the signal and output of it produces control signals that have important role in high performance because of its crossing point. In this paper the structure of the latch is reviewed. After considering the architecture of the latch, high performance latch with 0.18 µm technology is designed. It has high performance and improves dynamic parameter in data converter.

Key words: latch, inverter, switch, control signal, crossing point.

1. Introduction

The basic block in many applications to design mixed mode circuit is latch. Latch uses to keep the information. When the clock pulse applies, information goes to output. The input of latch is digital information. The output of the latch is control signals that apply to switches or transistors. The two important input of the latch is digital signal and clock pulse. If there are two switches with two phases, the control signal is very important to turn on or turn off the switches. Latch has two modes. When the clock pulse is high, input signal go to output, this mode call transport mode. When the clock pulse is low, the output is constant. This mode call hold mode. The latch designs with two NOT gates (two inverters). This article discusses how to design two outputs latch. First review conventional latch in part 2, then the suggested latch describes in part3. The simulation result is in part4 and part 5 is conclusion.

2.conventional latch

Figure 1 shows the inverter and transistor level. The inverter consists of PMOS transistor and NMOS transistor which PMOS puts in pull up network and NMOS transistor puts in pull down network. If the zero logic applies in to the inverter, the PMOS transistor is turn on and NMOS transistor is turn down. The output connects to power supply and become one logic. If the one logic applies to inverter, the PMOS transistor become off and NMOS transistor becomes on, then the output connect to ground and become zero.

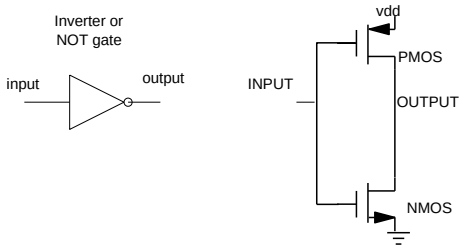

Fig 1: inverter.

Therefore if zero logic is input, the output is one. The input is logic one, the output is zero. In the design of inverter is chosen the symmetric inverter to better performance. In .18µm technology, µp * Cox is 60 µA/V^2 and µn* Cox is180 µA/V^2. µn is mobility of electrons and µp is mobility of holes. Cox is oxide gate capacitance. Therefore if two inverters are fastening back to back is making a latch. In figure 2, if the input is zero, the output is one. If the input is one, the output is zero logic. Figure 2 shows the transistor level of basic Latch.

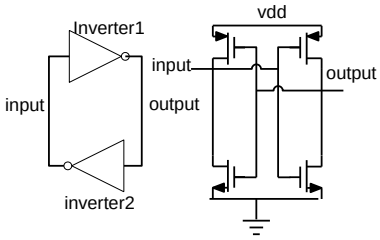

Fig 2: Basic Latch with transistor level.

The latch works with clock pulse. Figure 3 shows the figure 2 with clock pulse. When clock pulse is high, transistor M1, transistor M2 become on and the information enter to latch.

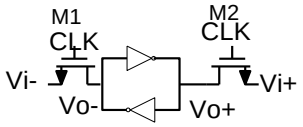

Fig 3: Latch with clock pulse.

Latch keeps the information until applies the clock pulse. Figure 4 shows the transistor level of figure 3. Figure 3 can use but no precision and performance. The logic in output can change, because the intrinsic capacitance of transistor can affect it.

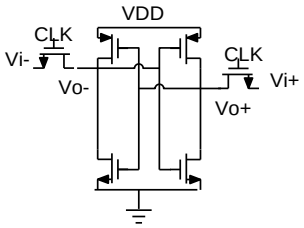

Fig 4: transistor level of fig 3.

3. propose latch

Try to change the structure of figure 4 to achieve the high performance latch to use in industry. First, put the inverter1 and inverter2. They fasten back to back to obtain figure 5. The reason to put the inv1, inv2 to keep the logic to apply in inverter3 (transistor M1, transistor M5) and inverter4 (transistor M4, transistor M6). In figure 5 the precision of input of inverter3 and inverter4 high because inverter1 and inverter2 make the latch and keep the information. Second, put transistor M2, transistor M3 to increase the precision of output. In figure 5, when the clock pulse is high, transistor MCLK1 and transistor MCLK2 is on, if one logic applies to VI- and zero logic applies to VI+, VO+ is zero logic and VO- is one logic, therefore Transistor M3 is on and VO- connects to VDD to keep one logic. Transistor M2 is off and VO+ is zero logic.

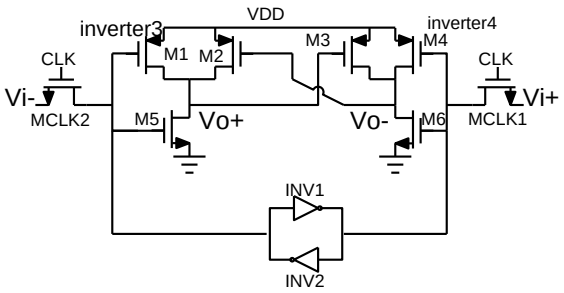

Fig 5: high performance latch.

Finally, the figure 6 shows the proposed latch. Use inv5, inv6, inv7 and inv8 to set up the crossing point of latch.

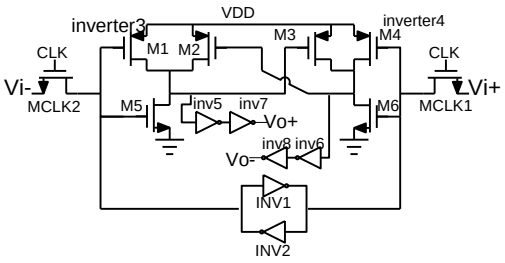

Fig 6: propose latch.

4. Results and Analysis

The duty of latch is produce the control signal. The important parameter is crossing point. Figure 7 and figure 8 shows the negative and positive control signal applies to switch or transistor. If one switch turn on sooner and second one turn off later, the performance of the system is poor. If the voltage of crossing point is VDD/2, VDD is voltage reference, both of the switches or transistors are off. The place of crossing point is chosen lower than VDD/2. In the outputs of latch use two inverter in any branch that inverter5 and inverter7 go raise the crossing point upper than VDD/2. The size of PMOS transistor is chosen bigger than NMOS transistor. Inverter6 and inverter8 invert the position of crossing point that lowers than VDD/2. The size of NMOS transistor is chosen bigger than PMOS transistor to reach the optimum point that latch do well. Figure 9 shows the crossing point

of the two outputs of the latch. Figure 10 shows the spectrum of D/A (Digital to Analog Converter) to measure SFDR (Spurious Free Dynamic Range).

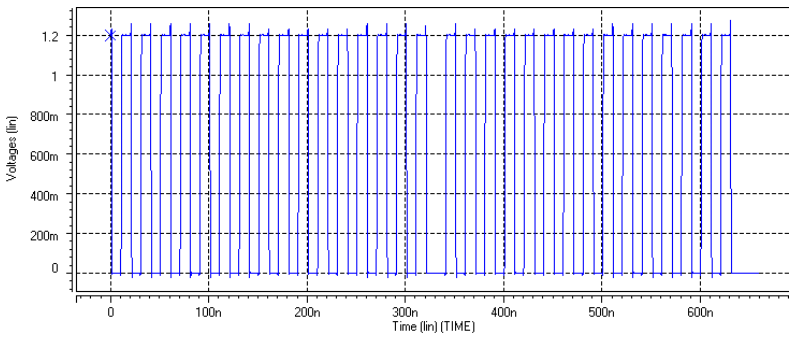

Fig 7: negative control signal.

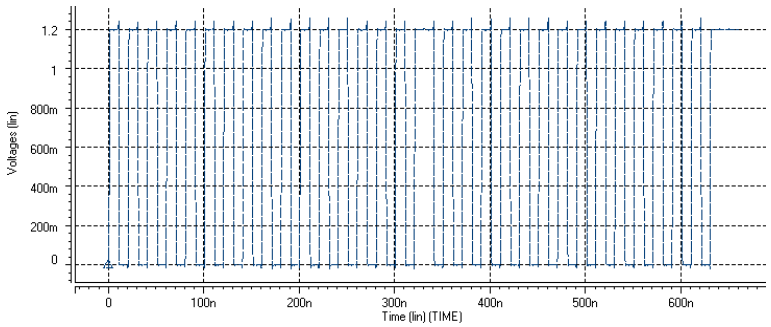

Fig 8: positive control signal.

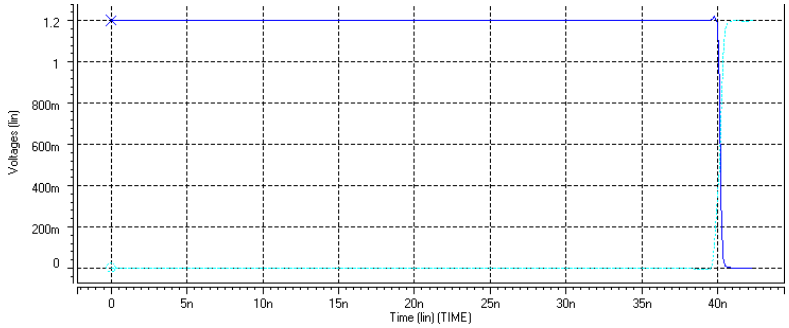

Fig 9: crossing point of the latch.

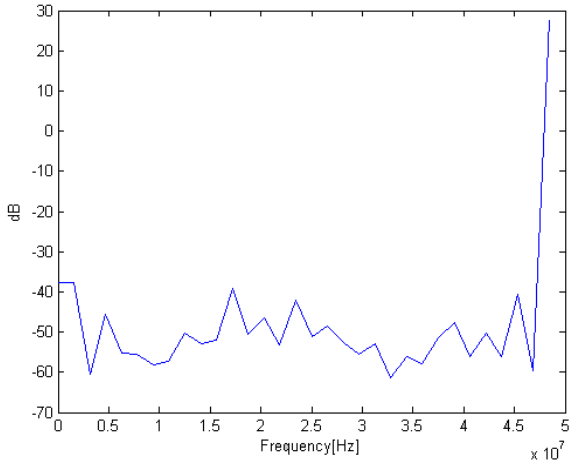

Fig 10: the spectrum of D/A

5. Conclusions

This paper tries to achieve the high performance latch for high speed application. This latch has two inputs and outputs. The control signals and crossing point of the latch affect the circuit and system. To reach the high performance and define the crossing point figure 6 is proposed. This latch in data converter is tested and is improved the performance of the system. The latch increases the SFDR parameter of D/A. The D/A converter is 10 bit and clock frequency is 100 MHZ. The input frequency 48.43 MHZ applies to D/A. In figure 10, SFDR is 65.481 dB. This latch works until 1 GHZ frequency. It deigns in 0.18 µm technology. The power supply for it is 1.2 volt. It consumes low power dissipation.

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