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Designing of a digital to analog convertor fully in CMOS ,0.18µm ,1.8V technology with SFDR more than 70dB

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Abstract

Nowadays in New system of communication, analog to digital and digital to analog converters are used plenteously. Digital to analog converters are converters that receive digital data and convert it to an analog signal. We can compound different methods of designing different parts of digital to analog converters to achieve to complex designing. complex designings are very common methods in converters designing because compound different methods points. In this article we design and simulate a digital to analog converter .This converter receive 6 low-worth first bits in the form of binary and 4 worthy last bits in the form of unary thermometer codes. Output of this converter is in the form of sinusoidal signal .This converter has high amounts of SNR and SFDR.

Key words: converter, digital, analog, unary thermometer code

1. Introduction

This article deal with say acquired result of a research about design , simulation and survey performance of a digital to analog converter that is designed in the complex form. Nowadays in New system of communication, analog to digital and digital to analog converters are used plenteously. Analog to digital converters are converters that receive analog data and convert it to digital signal and Digital to analog converters are converters that receive digital data and convert it to analog signal. There are different methods to design digital to analog converters and each method has its benefits and sins. We can compound different methods of designing different parts of digital to analog converters to achieve to complex designing. complex designings are very common methods in converters designing because compound different methods points.[1],[6] Frequency mutation decreased much with unary thermometer code method for MSBs(worth bits) and with binary size method for LSBs and accuracy is obtained for worthy bits that are most in need. However in part of low, worthy bits the matter of mutation and accuracy is included less but worthy frugality in the level of binary method is done. In continuation we deal with expression of demands and design of converter.[1],[2],[5]

2. Design

1-2. expression of design demands

Purpose is designing of a digital to analog converter fully in CMOS, 0.18µm, 1.8V technology with following specifications:

- Resolution: 10-bit
- SFDR>70dB (f_{clk} = 150MSPS,$f_{out\text{-}max}=(k/m)f_{clk}$, k = 256 , M = 4096)
- The digital sinusoidal input should scan all possible codes

In design the DAC according to figure 1should be performed 6 low-worth first bits in the form of binary and 4 worthy last bit in the form of unary thermometer code. We most select current source from cascade type as figure 2.

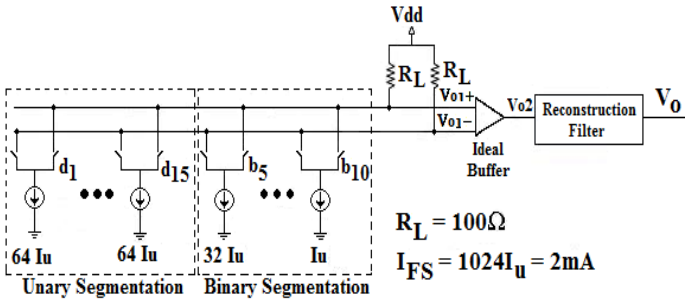


Fig1: scheme of the digital to analog converter that is wanted to design

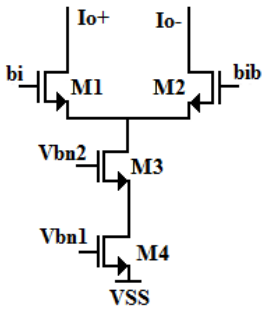


Fig 2: scheme of the cascade current source that is used in to digital to analog converter of figure 1

2-2. Current source design

At first we should design current source to start . In the first place we determine amount of W and L according to transistors performance in accordance with figure 2.
For this according to said technology we have:

L=0.18µm
For M1 and M2 transistors that have key role in circuit ,we consider $M_1$and M_2 amounts as below , because these transistors should be able to transmit most current .

W1= 1.8 µm

W2=1.8 µm

M_3 and M_4 transistors are current generators so amount of W/L should be low as possible as to be able to generate much current . Regarding this matter we consider W_3 and W_4 amount as below .
W_3=0.36µm
W_4=0.36µm

Now with knowing these amounts and supposing M3 and M4 transistors do at saturation area , we calculate V_{bn1} and V_{bn2} voltages manually to have intended I_u current . Then we write a netlist file with manual calculations results and design V_{bn1} and V_{bn2} with computer and Hspice software and with intended technology, result will be as:

V_{bn1}= 520mV
V_{bn2}= 580mV

3-2. Filter

In use filter in this project is a 3 stage Butter worth filter with Sallen Key format. If we design filter to have 10MHz cut-off frequency, filter specifications are such az table 1 and its scheme is such as figure3.[3]

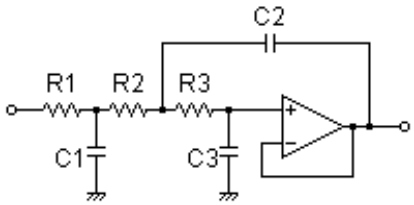
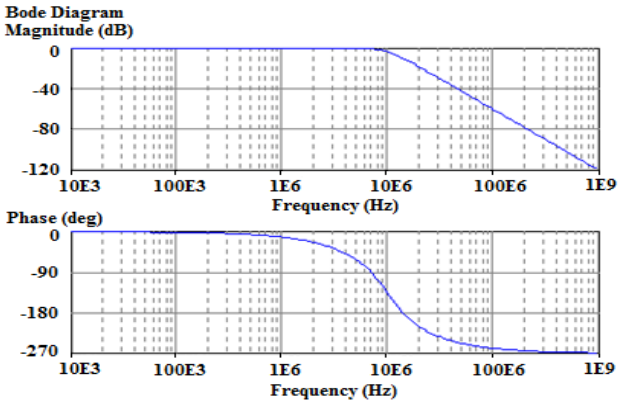


Fig3: scheme of the 3 stage Butter worth filter with Sallen Key format

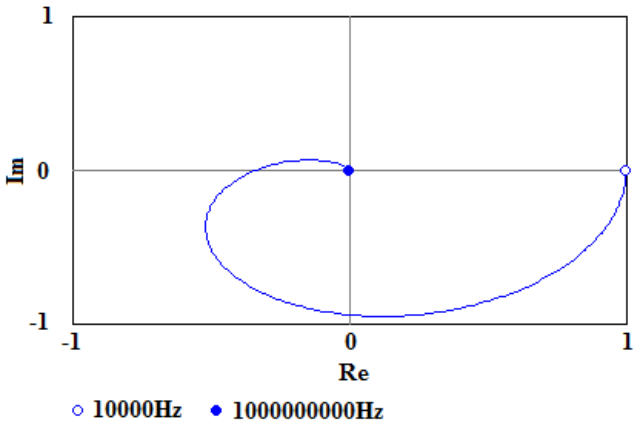
element	amount	element	amount
R1	11kΩ	C1	1.5PF
R2	110kΩ	C2	0.68PF
R3	33kΩ	C3	0.1PF

TABLE 1.AMOUNT OF ELEMENTS OF FIGURE2

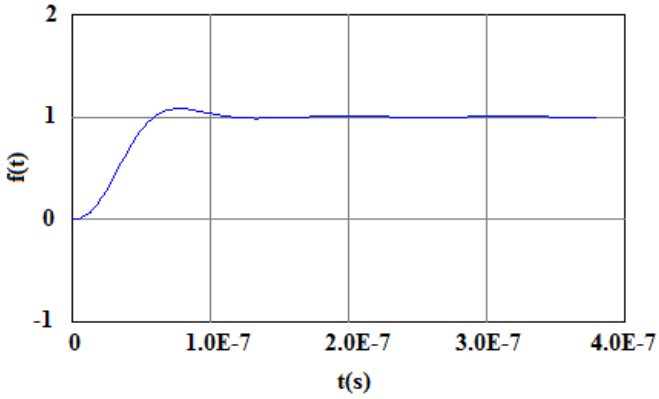
The Bode diagram , Nyquist diagram and step response of the Fillter of figure 3 are such az figure4.



a) Bode diagram



b) Nyquist diagram



c) step response

Fig4: a)Bode diagram, b)Nyquist diagram & c) step response of the 3 stage Butter worth filter with Sallen Key format

4-2.Ideal buffer

Ideal buffer according to figure 5 has extreme incoming resistance, output resistance equal Zero and unit gain. In this project we associate ideal buffer with a voltage depended voltage source wherein[4]:

$R_{in}=\infty$
$R_{out}=0$
G=1

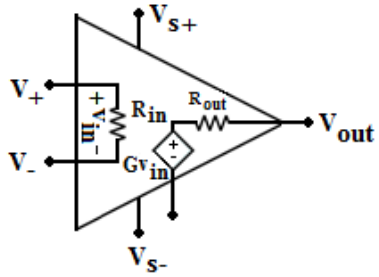


Fig5: Ideal buffer

5-2.Design of digital to analog converter

In previous part we introduced and design different parts of digital to analog converter of figure 1. Here we want to design and simulate circuit of figure 1 with designed parts in previous parts. For this we use Hspice 2008 software. For design and simulation we should notice that in each part of circuit regarding index of I_u must have as number of current sources. For example in unary segmention part from d_1 to d_{15}, current source is used 15 times that each time regarding index of I_u is equal with 64, so we should use current source 64 times.

For generation of entrance signal, we consider two DC voltage source that connect in one way to current source entrances and in other way to the ground and discrib them for d_1 to d_{15} and b_5 to b_{10} . amount of these DC sources in each time is very our digital codes. We discibe these sources with a digital sinusoidal function that can cover all of the possible codes. For example figure 6 and figure 7 respectively are related to d1, d1b and b5 , b5b entrances.

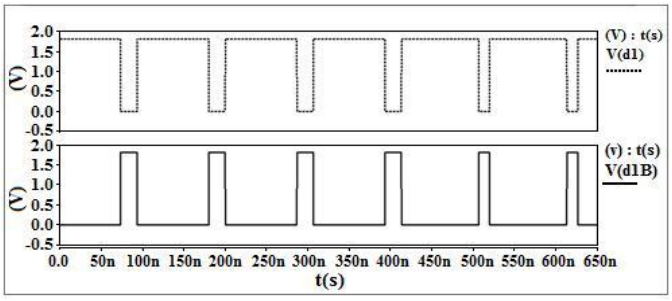


Fig6: Digital signal of d1 and d1b entrances.

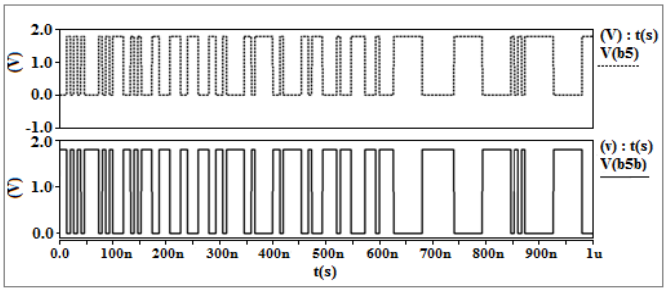


Fig7: Digital signal of b5 and b5b entrances

The gain of used buffer in circuit equal 1, then we select transient analysis type and use .PRINT and .PROB orders to print and draw output voltage. Wave forms of output voltage before filter (V_{o2}) and after the filter (V_o) will be as figures 8 and 9.
Notic that incoming digital signal has converted to a sinusoidal signal.

6-2.Calculation of SNR and SFDR

We take related data of voltage of output node (V_o) and then calculate related amount of SNR[1] and SFDR[2] with Matlab software. Figure 10 is related to calculation of SFDR that has got with Matlab software. Amount of SNR and SFDR are equal with:

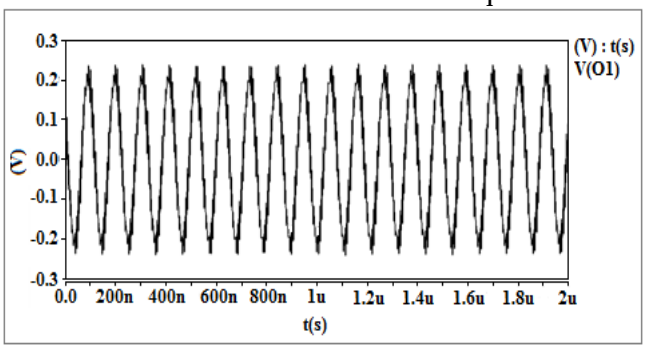


Fig8: Wave forms of output voltage before filter (V_{o2})

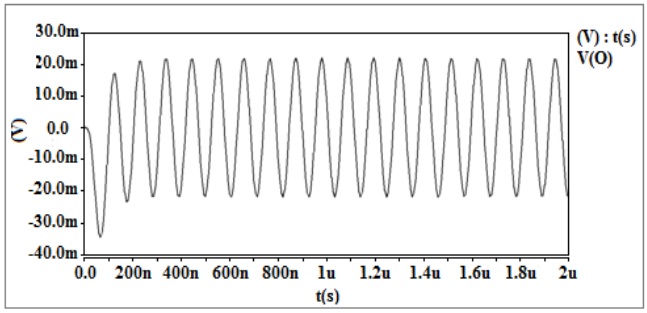


Fig9:Wave forms of output voltage before filter (V_{o2})

SNR=61.7590dB
SFDR=73.3218dB

[1] - signal to noise ratio
[2] - spurious free dynamic rang

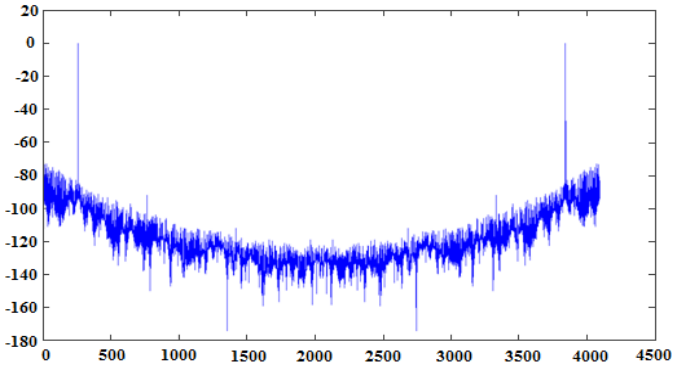


Fig10:Wave forms for calculation of SFDR

3. Conclusion

In past, different digital to analog converters has designed with different characteristics[7]. But designed converter ofthispaper is in kind of complex digital to analog converters.

We notice that amounts of SNR and SFDR of the digital to analog converter of figure 1 are respectively 61.75dB and 73.32dB that both of them are considerable and even are more than wanted amount in design conditions.
It's outpot is in the form of sinusoidal without distortion too. The reason of this matter is using filter in output of circuit.
Totally as we had also said, mixed designs are very common methods in design of converters, because they compound different methods points.[1],[2]

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